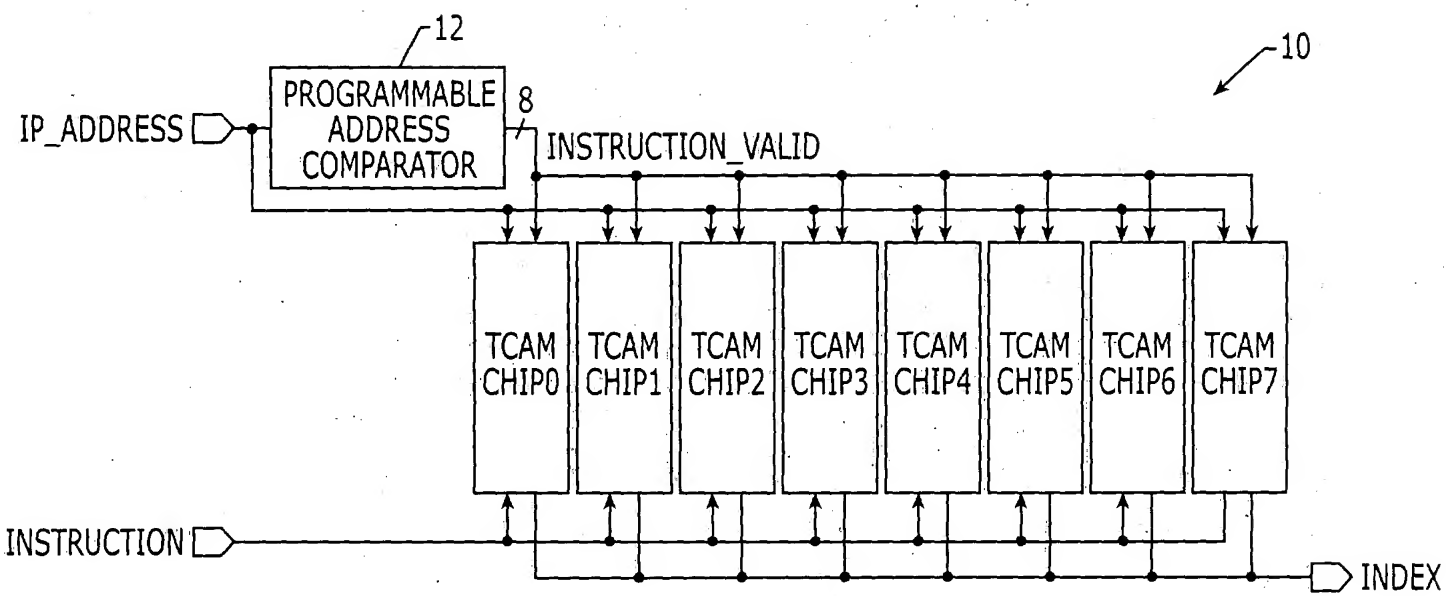


FIG. 1A
(PRIOR ART)

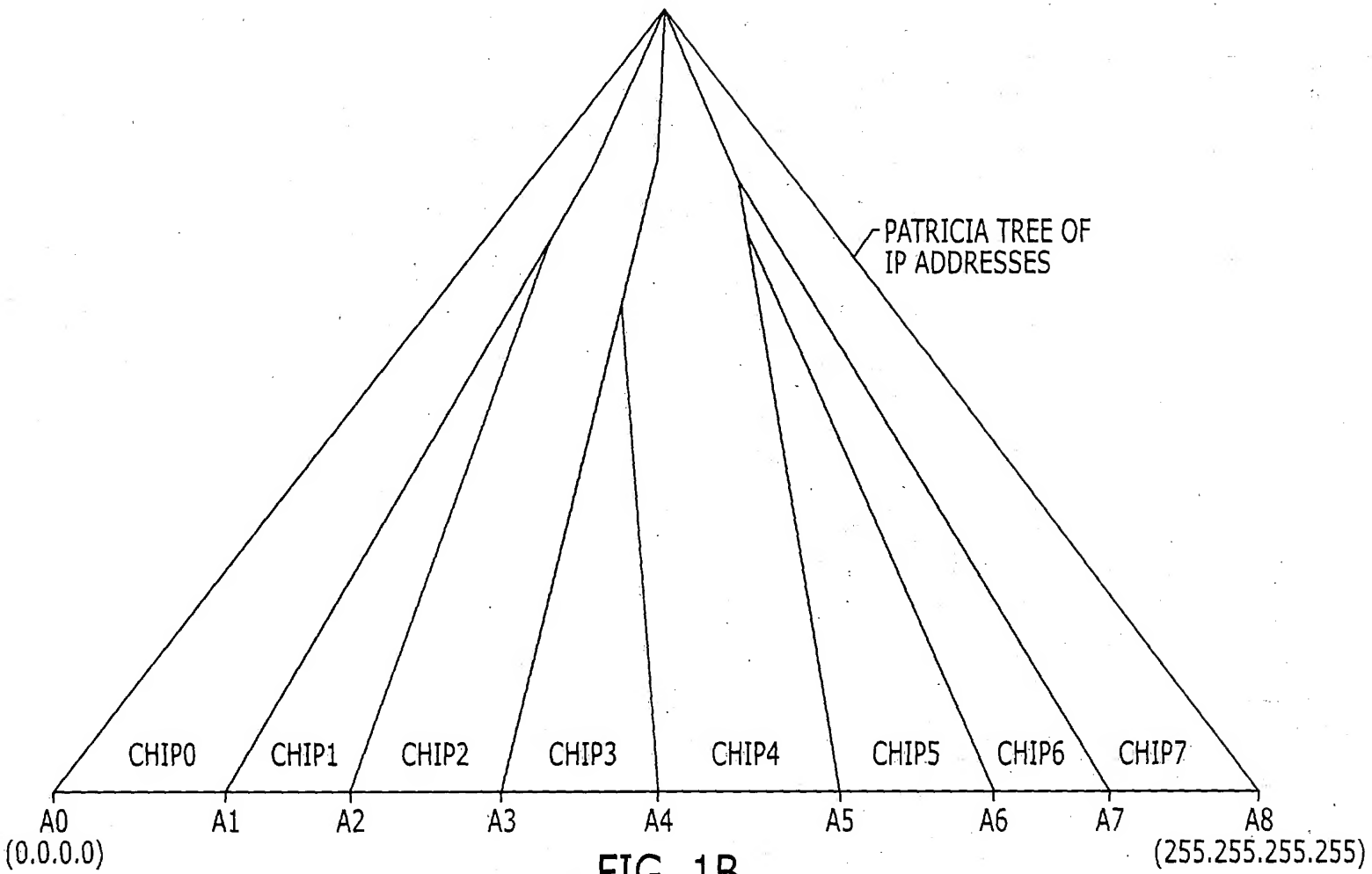


FIG. 1B
(PRIOR ART)

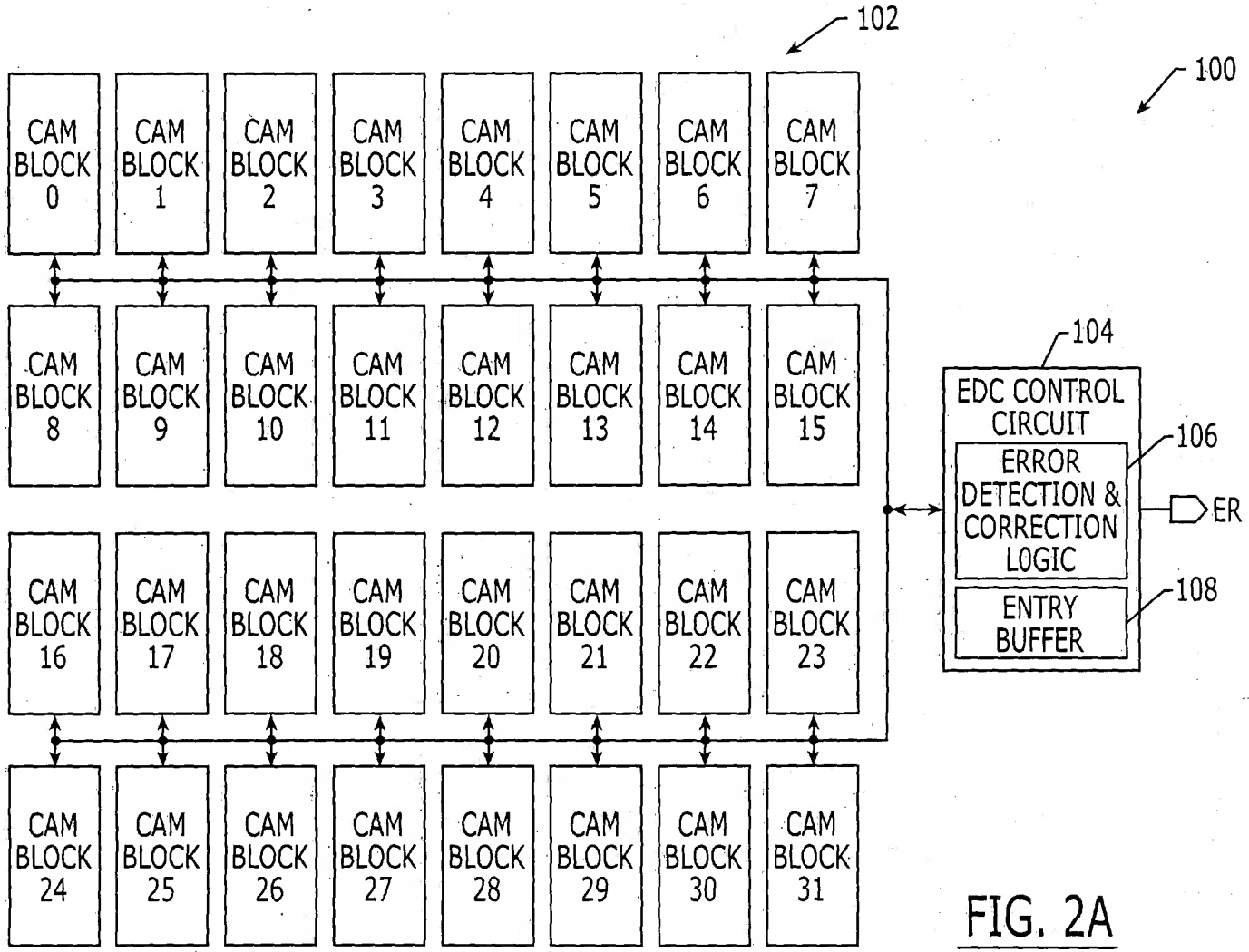
102
100
CAM BLOCK 0
CAM BLOCK 1
CAM BLOCK 2
CAM BLOCK 3
CAM BLOCK 4
CAM BLOCK 5
CAM BLOCK 6
CAM BLOCK 7
CAM BLOCK 8
CAM BLOCK 9
CAM BLOCK 10
CAM BLOCK 11
CAM BLOCK 12
CAM BLOCK 13
CAM BLOCK 14
CAM BLOCK 15
CAM BLOCK 16
CAM BLOCK 17
CAM BLOCK 18
CAM BLOCK 19
CAM BLOCK 20
CAM BLOCK 21
CAM BLOCK 22
CAM BLOCK 23
CAM BLOCK 24
CAM BLOCK 25
CAM BLOCK 26
CAM BLOCK 27
CAM BLOCK 28
CAM BLOCK 29
CAM BLOCK 30
CAM BLOCK 31
104
EDC CONTROL CIRCUIT
106
ERROR DETECTION & CORRECTION LOGIC
ER
108
ENTRY BUFFER

FIG. 2A

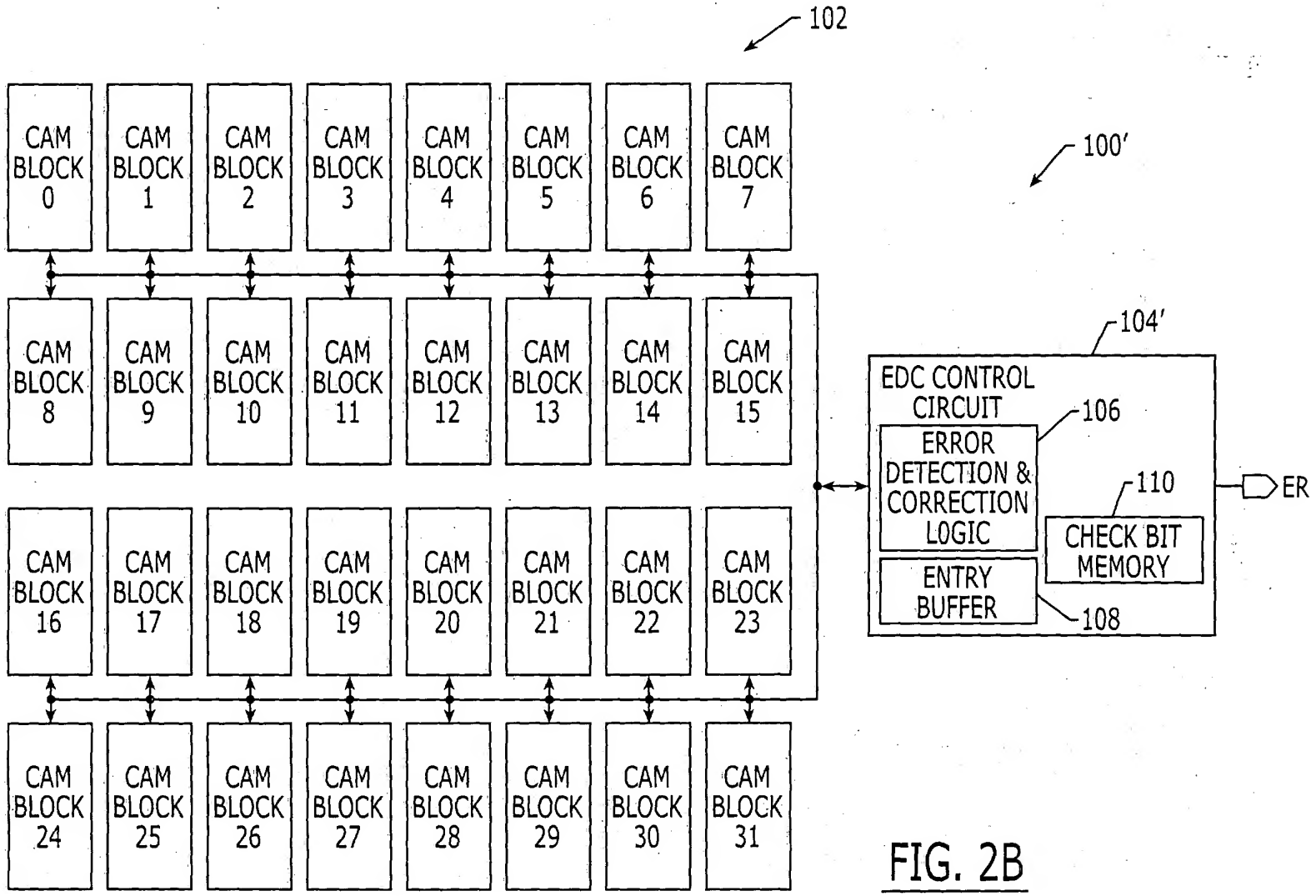
102
100'
CAM BLOCK 0
CAM BLOCK 1
CAM BLOCK 2
CAM BLOCK 3
CAM BLOCK 4
CAM BLOCK 5
CAM BLOCK 6
CAM BLOCK 7
CAM BLOCK 8
CAM BLOCK 9
CAM BLOCK 10
CAM BLOCK 11
CAM BLOCK 12
CAM BLOCK 13
CAM BLOCK 14
CAM BLOCK 15
CAM BLOCK 16
CAM BLOCK 17
CAM BLOCK 18
CAM BLOCK 19
CAM BLOCK 20
CAM BLOCK 21
CAM BLOCK 22
CAM BLOCK 23
CAM BLOCK 24
CAM BLOCK 25
CAM BLOCK 26
CAM BLOCK 27
CAM BLOCK 28
CAM BLOCK 29
CAM BLOCK 30
CAM BLOCK 31
104'
EDC CONTROL CIRCUIT
106
ERROR DETECTION & CORRECTION LOGIC
110
CHECK BIT MEMORY
ENTRY BUFFER
108
ER

FIG. 2B

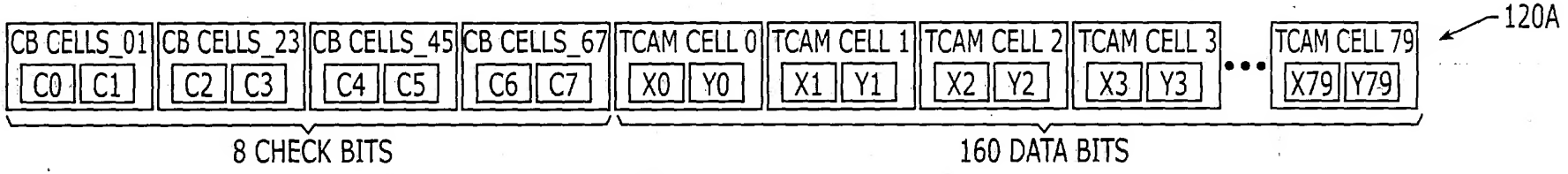


FIG. 3A

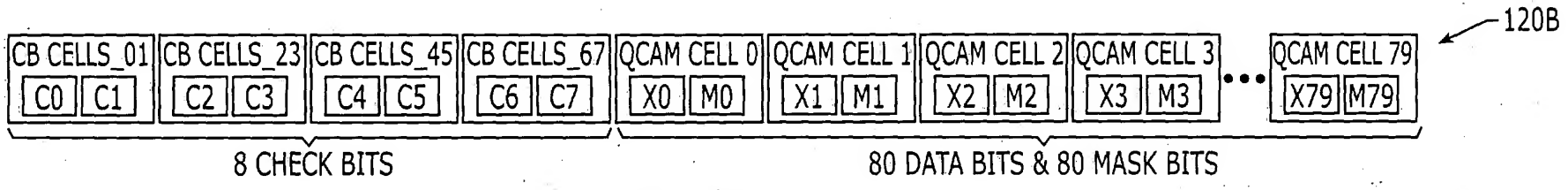


FIG. 3B

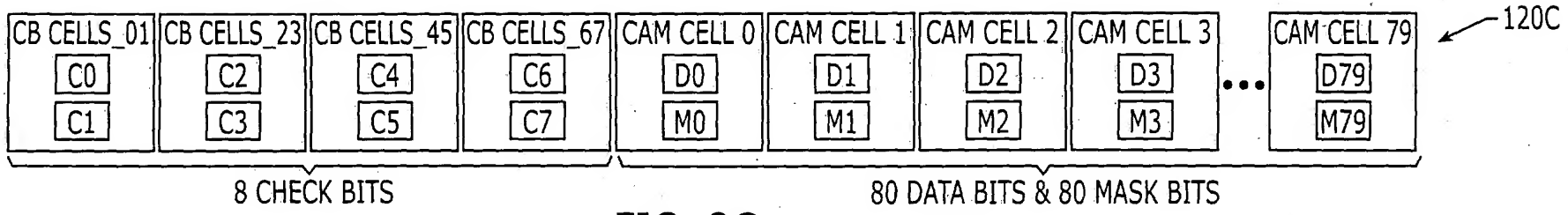


FIG. 3C

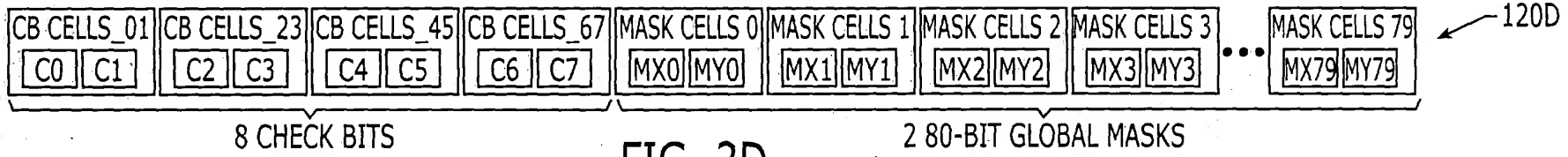


FIG. 3D

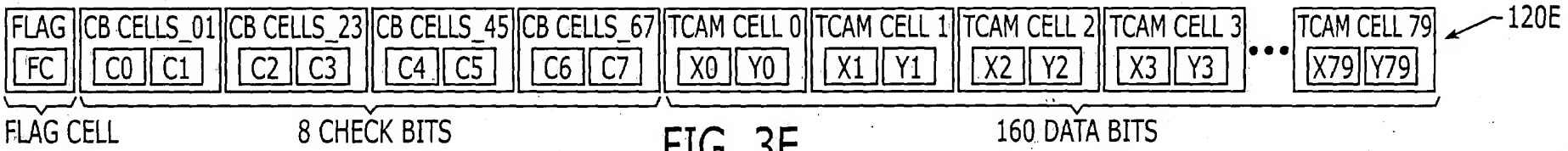


FIG. 3E

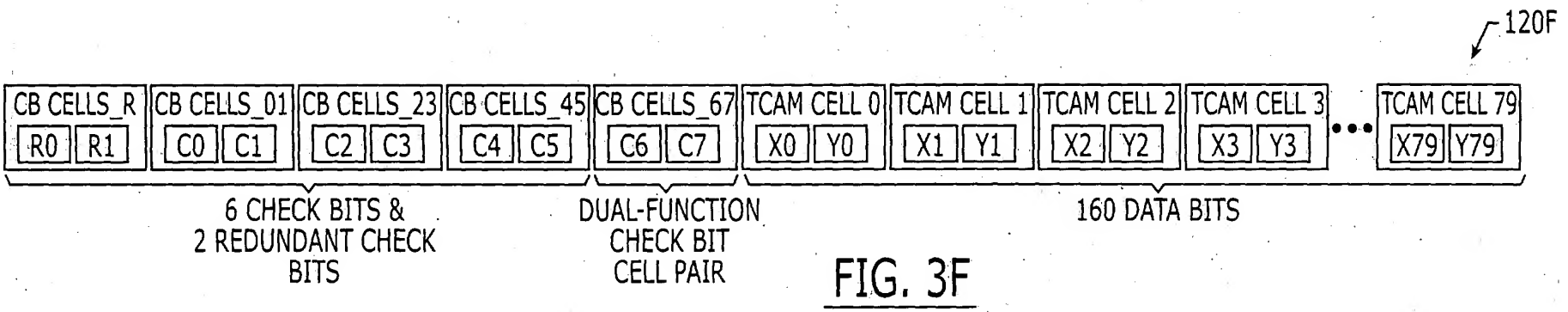


FIG. 3F

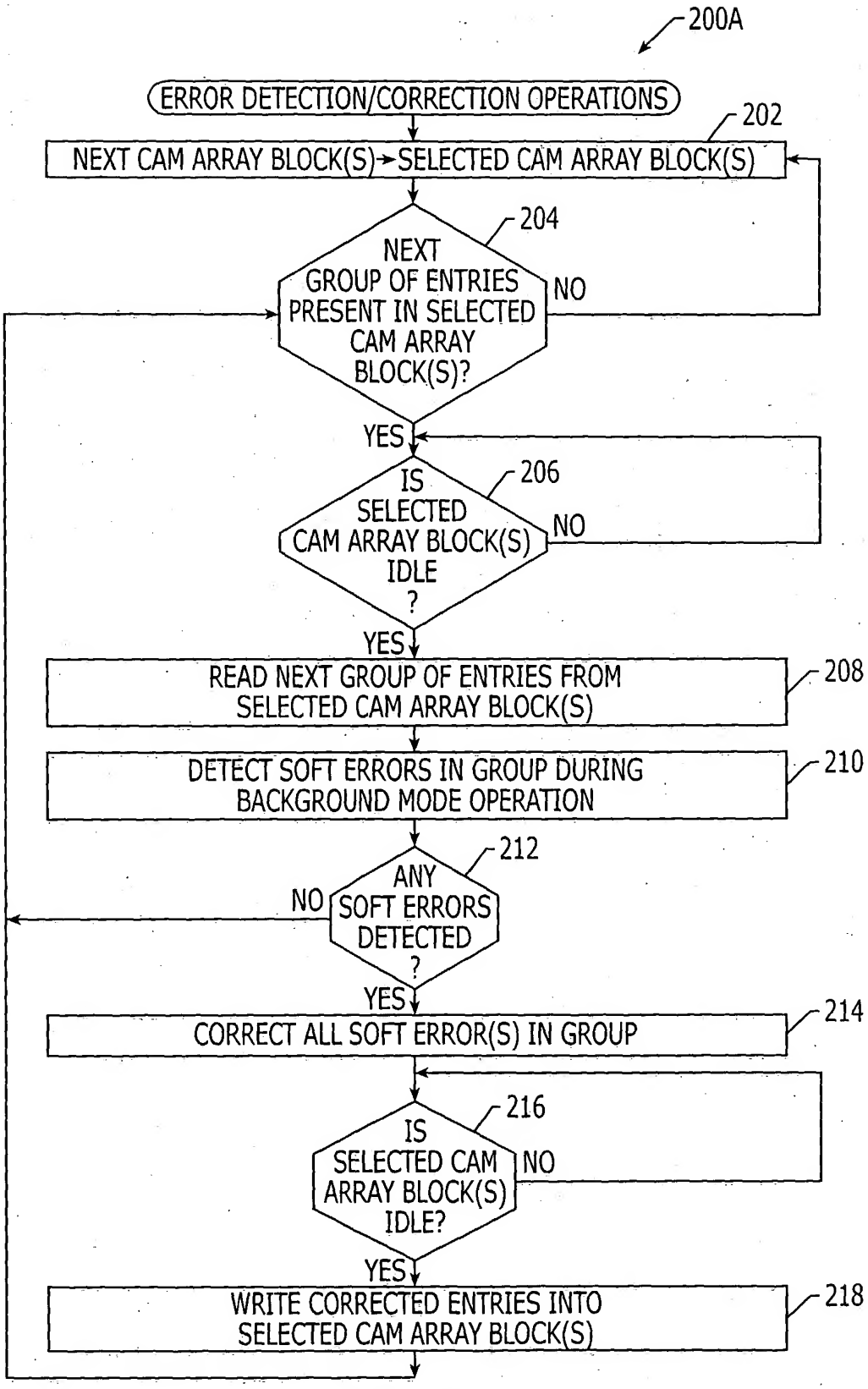
200A
ERROR DETECTION/CORRECTION OPERATIONS
202
NEXT CAM ARRAY BLOCK(S)→SELECTED CAM ARRAY BLOCK(S)
204
NEXT GROUP OF ENTRIES PRESENT IN SELECTED CAM ARRAY BLOCK(S)?
NO
YES
206
IS SELECTED CAM ARRAY BLOCK(S) IDLE ?
NO
YES
208
READ NEXT GROUP OF ENTRIES FROM SELECTED CAM ARRAY BLOCK(S)
210
DETECT SOFT ERRORS IN GROUP DURING BACKGROUND MODE OPERATION
212
ANY SOFT ERRORS DETECTED ?
NO
YES
214
CORRECT ALL SOFT ERROR(S) IN GROUP
216
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
218
WRITE CORRECTED ENTRIES INTO SELECTED CAM ARRAY BLOCK(S)

FIG. 4A

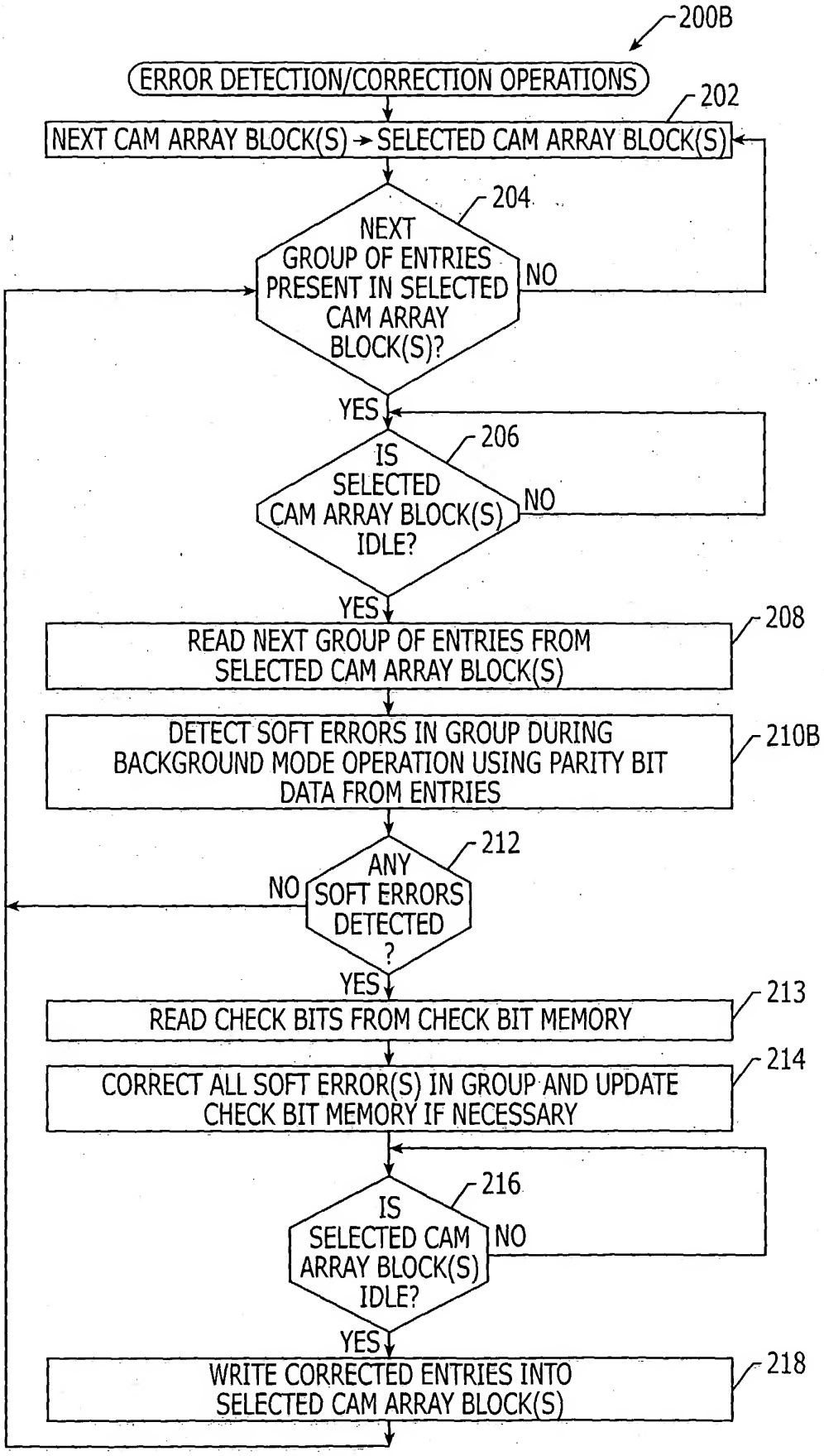
200B
ERROR DETECTION/CORRECTION OPERATIONS
202
NEXT CAM ARRAY BLOCK(S) → SELECTED CAM ARRAY BLOCK(S)
204
NEXT GROUP OF ENTRIES PRESENT IN SELECTED CAM ARRAY BLOCK(S)?
NO
YES
206
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
208
READ NEXT GROUP OF ENTRIES FROM SELECTED CAM ARRAY BLOCK(S)
210B
DETECT SOFT ERRORS IN GROUP DURING BACKGROUND MODE OPERATION USING PARITY BIT DATA FROM ENTRIES
212
ANY SOFT ERRORS DETECTED ?
NO
YES
213
READ CHECK BITS FROM CHECK BIT MEMORY
214
CORRECT ALL SOFT ERROR(S) IN GROUP AND UPDATE CHECK BIT MEMORY IF NECESSARY
216
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
218
WRITE CORRECTED ENTRIES INTO SELECTED CAM ARRAY BLOCK(S)

FIG. 4B

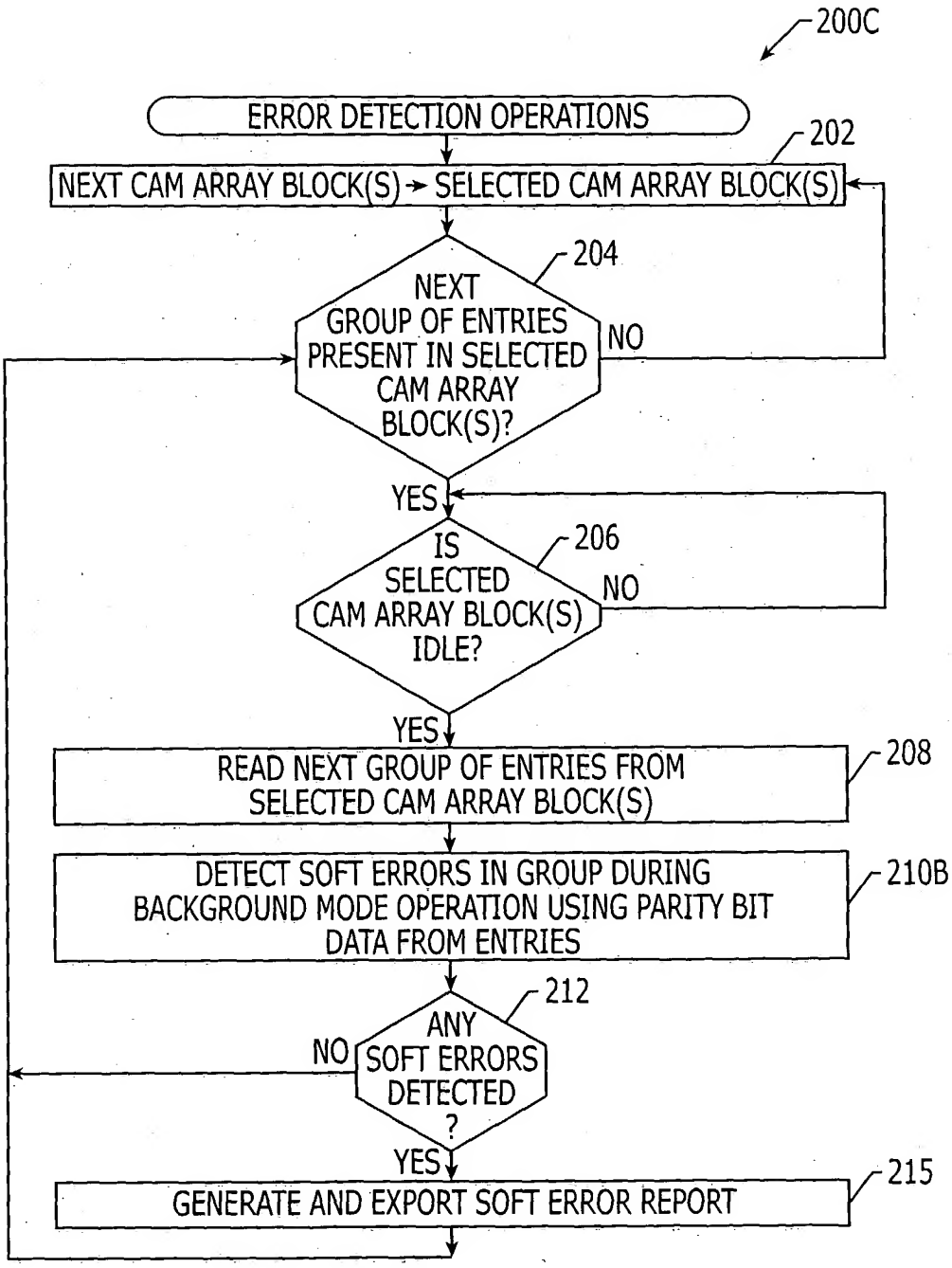
200C
ERROR DETECTION OPERATIONS
202
NEXT CAM ARRAY BLOCK(S) → SELECTED CAM ARRAY BLOCK(S)
204
NEXT GROUP OF ENTRIES PRESENT IN SELECTED CAM ARRAY BLOCK(S)?
NO
YES
206
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
208
READ NEXT GROUP OF ENTRIES FROM SELECTED CAM ARRAY BLOCK(S)
210B
DETECT SOFT ERRORS IN GROUP DURING BACKGROUND MODE OPERATION USING PARITY BIT DATA FROM ENTRIES
212
ANY SOFT ERRORS DETECTED ?
NO
YES
215
GENERATE AND EXPORT SOFT ERROR REPORT

FIG. 4C

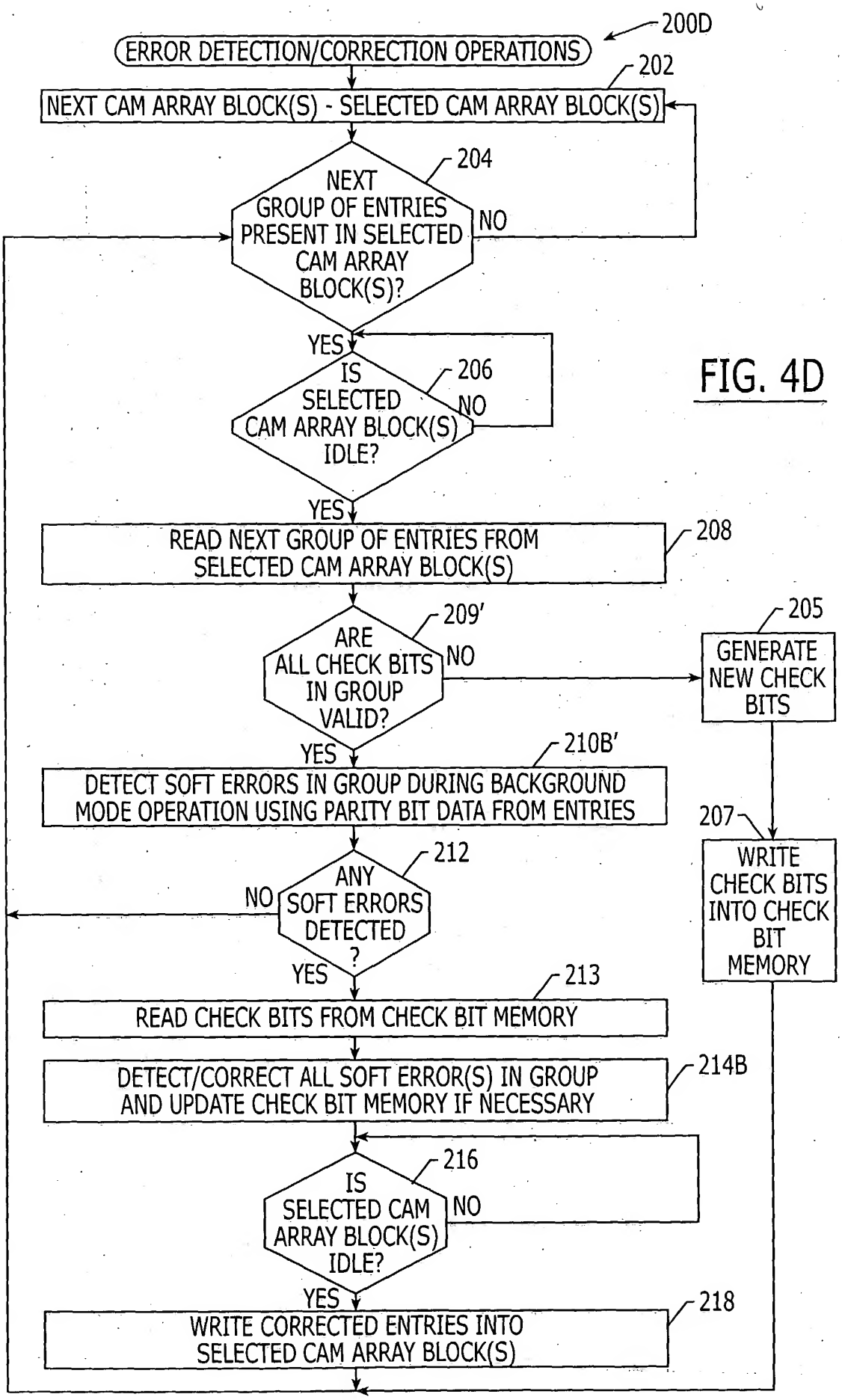
200D
ERROR DETECTION/CORRECTION OPERATIONS
202
NEXT CAM ARRAY BLOCK(S) - SELECTED CAM ARRAY BLOCK(S)
204
NEXT GROUP OF ENTRIES PRESENT IN SELECTED CAM ARRAY BLOCK(S)?
NO
YES
206
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
208
READ NEXT GROUP OF ENTRIES FROM SELECTED CAM ARRAY BLOCK(S)
209'
ARE ALL CHECK BITS IN GROUP VALID?
NO
205
GENERATE NEW CHECK BITS
YES
210B'
DETECT SOFT ERRORS IN GROUP DURING BACKGROUND MODE OPERATION USING PARITY BIT DATA FROM ENTRIES
207
WRITE CHECK BITS INTO CHECK BIT MEMORY
212
ANY SOFT ERRORS DETECTED ?
NO
YES
213
READ CHECK BITS FROM CHECK BIT MEMORY
214B
DETECT/CORRECT ALL SOFT ERROR(S) IN GROUP AND UPDATE CHECK BIT MEMORY IF NECESSARY
216
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
218
WRITE CORRECTED ENTRIES INTO SELECTED CAM ARRAY BLOCK(S)

FIG. 4D

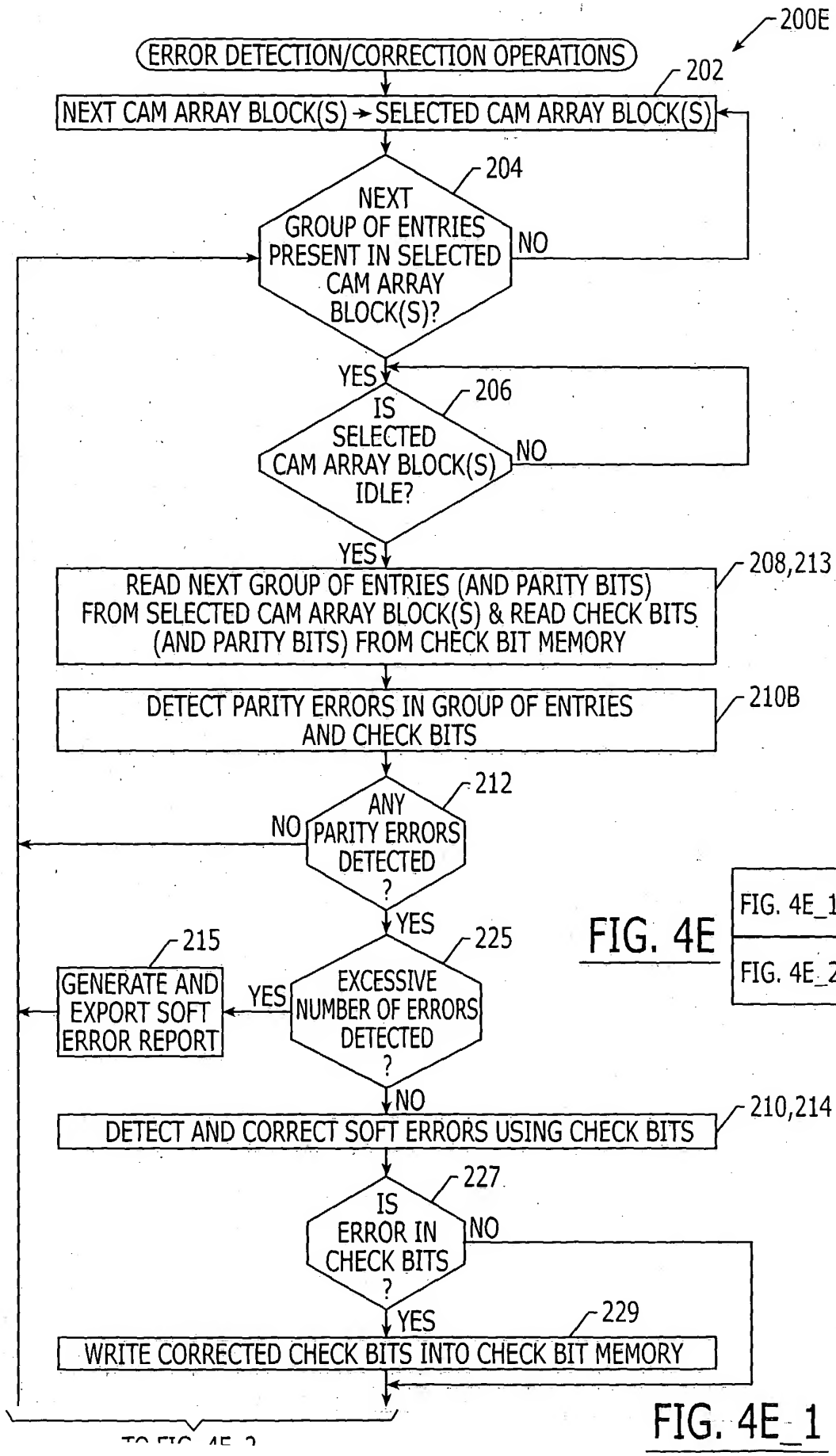


FIG. 4E

FIG. 4E_1
FIG. 4E_2

FIG. 4E_1

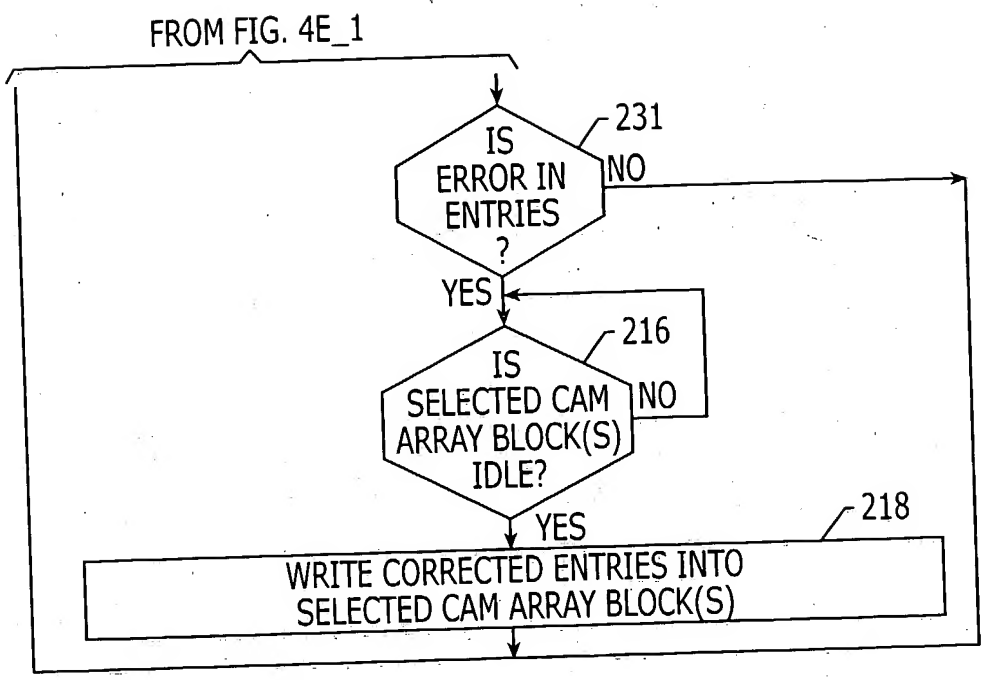
FROM FIG. 4E_1
IS ERROR IN ENTRIES ?
231
NO
YES
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
216
NO
YES
218
WRITE CORRECTED ENTRIES INTO SELECTED CAM ARRAY BLOCK(S)

FIG. 4E_2

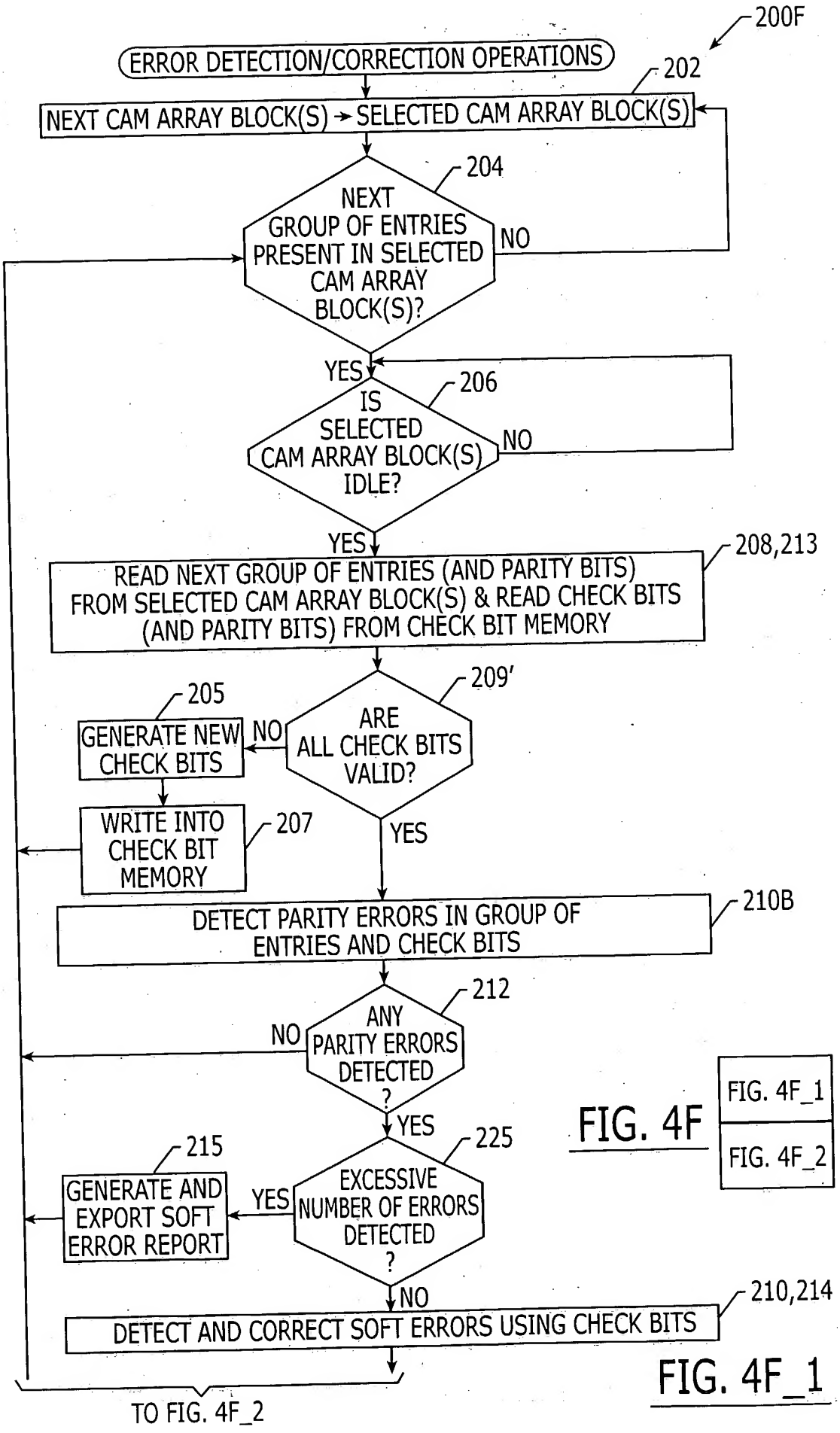


FIG. 4F_1

FIG. 4F

FIG. 4F_1

FIG. 4F_2

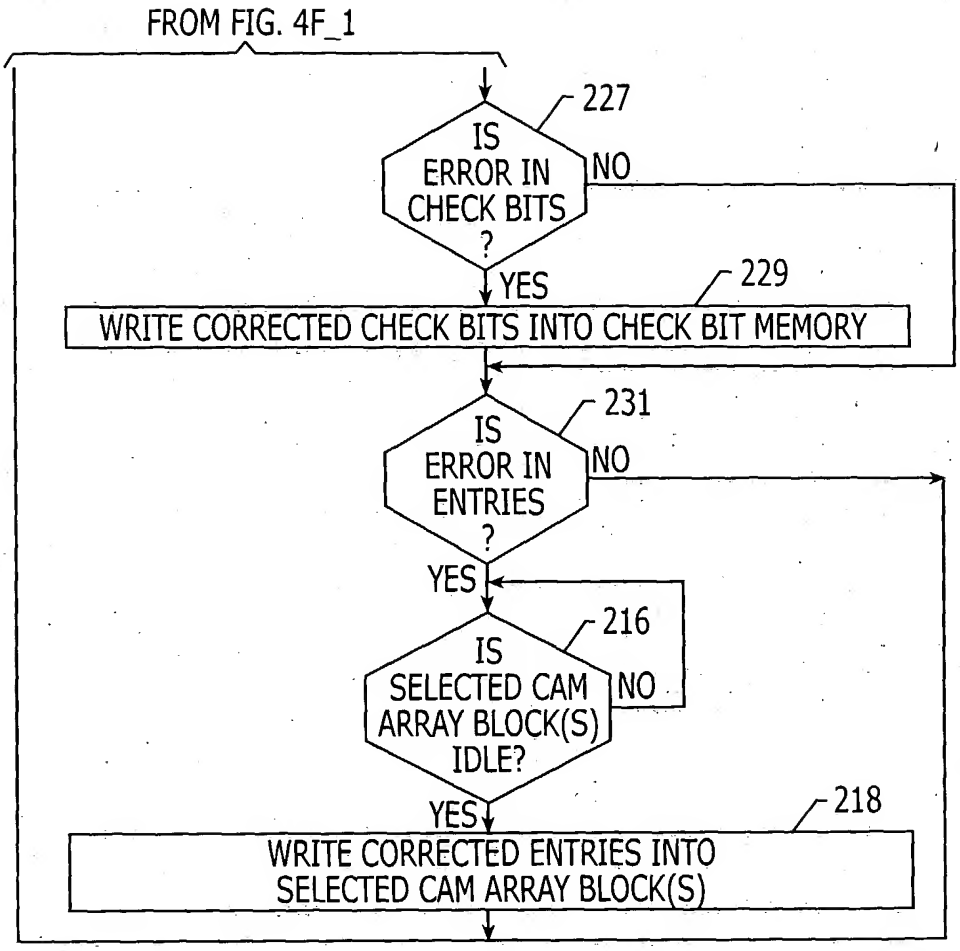
FROM FIG. 4F_1
227
IS ERROR IN CHECK BITS ?
NO
YES
229
WRITE CORRECTED CHECK BITS INTO CHECK BIT MEMORY
231
IS ERROR IN ENTRIES ?
NO
YES
216
IS SELECTED CAM ARRAY BLOCK(S) IDLE?
NO
YES
218
WRITE CORRECTED ENTRIES INTO SELECTED CAM ARRAY BLOCK(S)

FIG. 4F_2

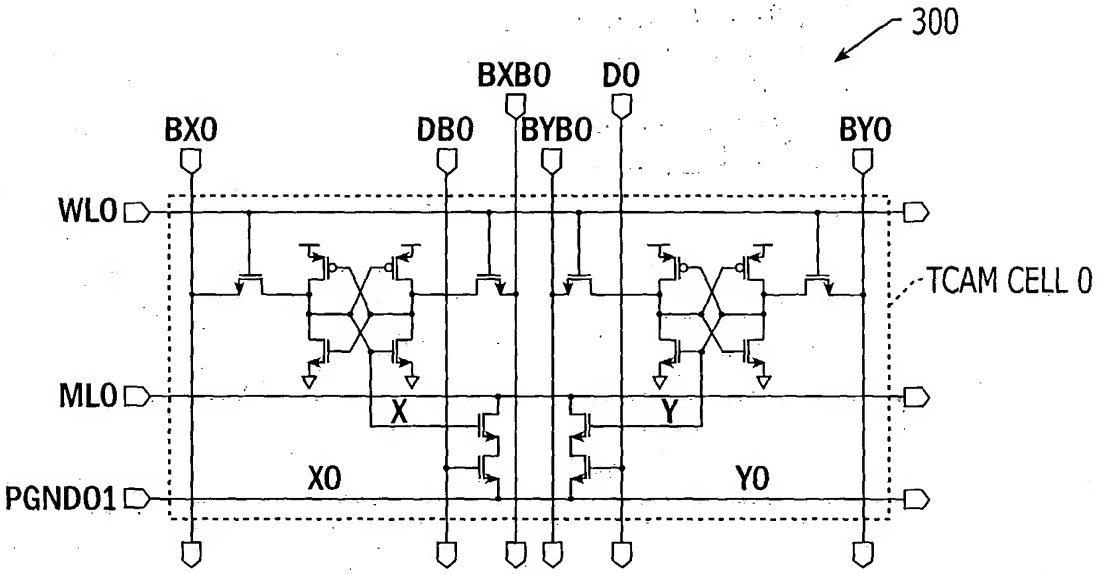


FIG. 5A

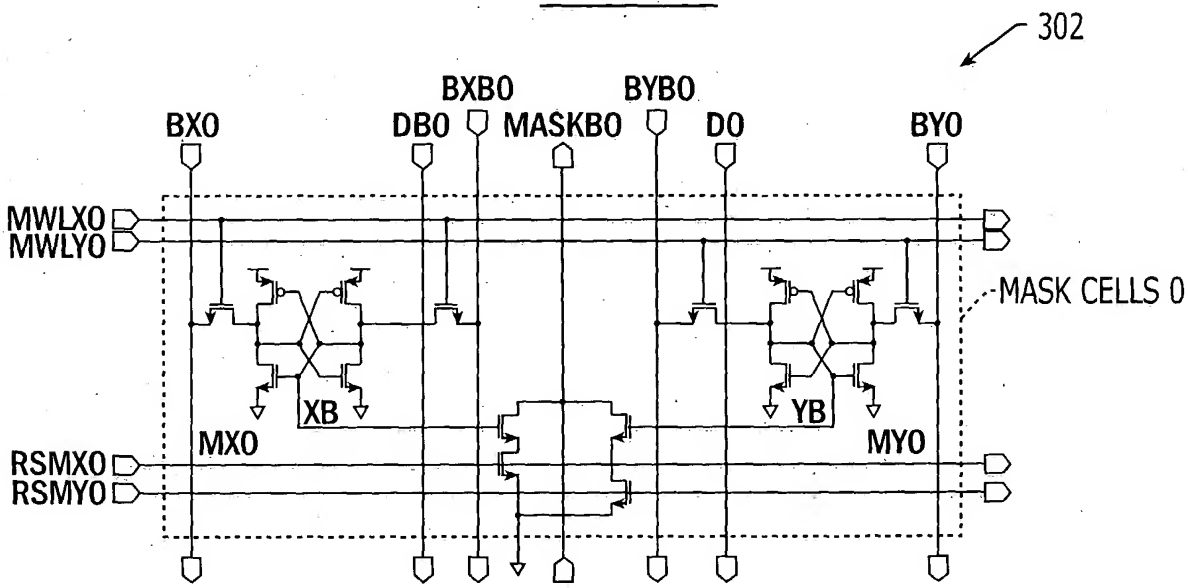


FIG. 5B

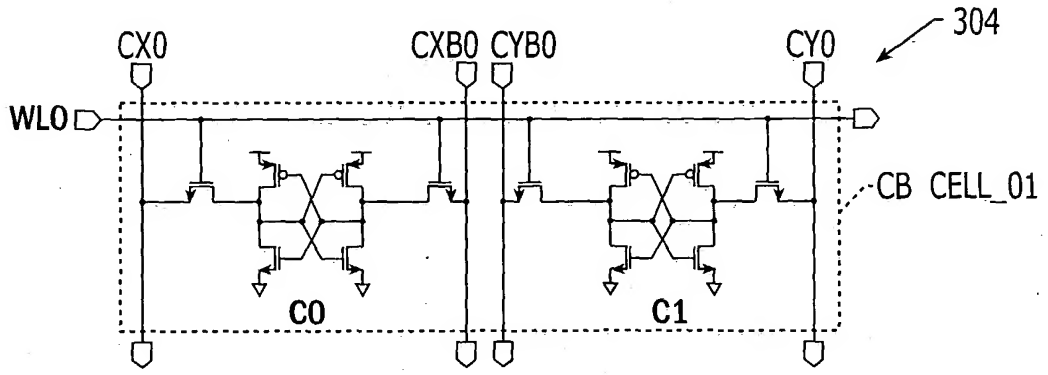


FIG. 5C

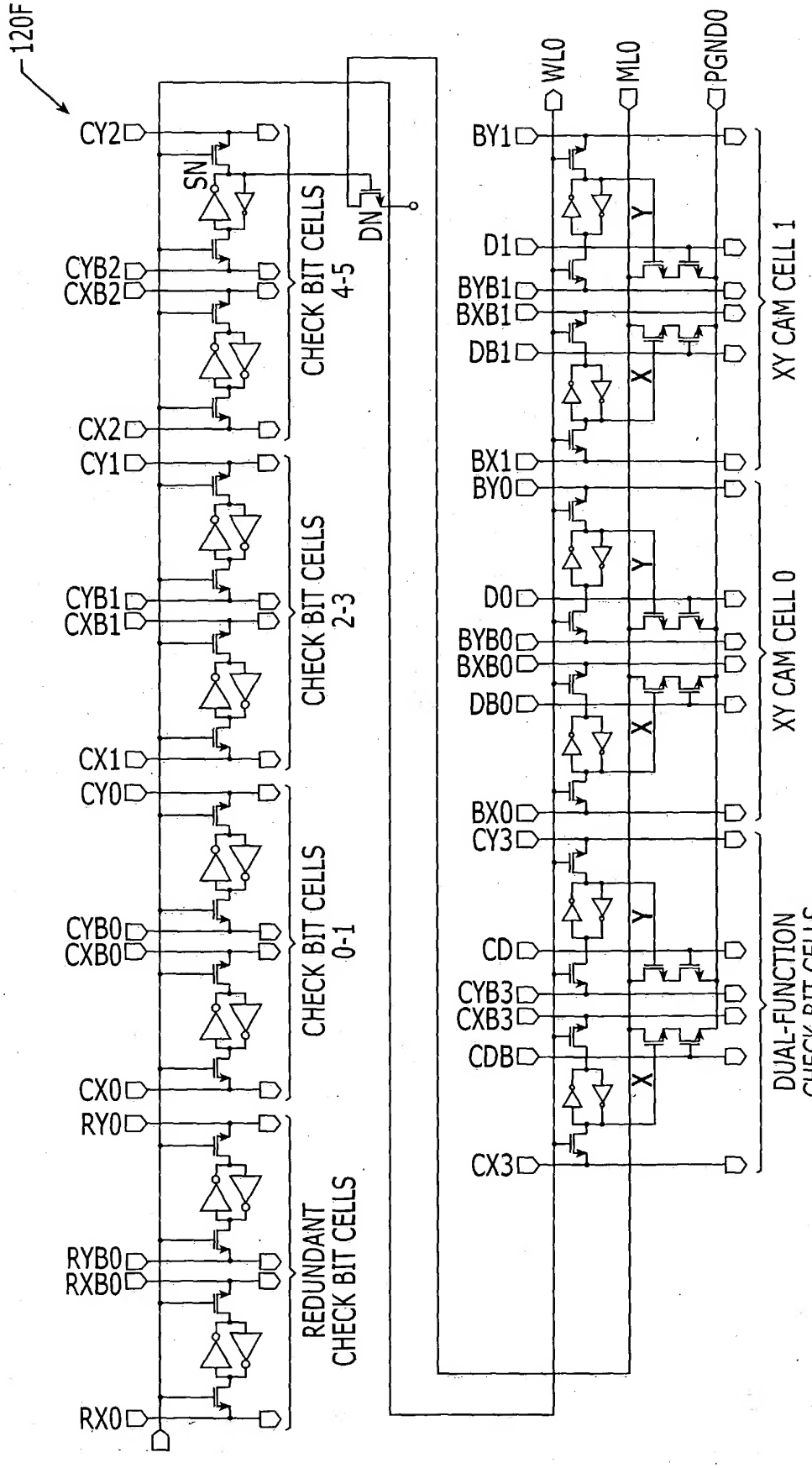
120F
CY2
SN
DN
CYB2
CXB2
CX2
CY1
CYB1
CXB1
CX1
CY0
CYB0
CXB0
CX0
RY0
RYB0
RXB0
RX0
CHECK BIT CELLS 4-5
CHECK BIT CELLS 2-3
CHECK BIT CELLS 0-1
REDUNDANT CHECK BIT CELLS
WL0
ML0
PGND0
BY1
D1
BYB1
BXB1
DB1
BX1
BY0
D0
BYB0
BXB0
DB0
BX0
CY3
CD
CYB3
CXB3
CDB
CX3
Y
X
XY CAM CELL 1
XY CAM CELL 0
DUAL-FUNCTION CHECK BIT CELLS 6-7

FIG. 6